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PATENT

TRICKLE CURRENT – CASCODE DAC

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of United States Provisional Application No. 60/480,987, filed June 20, 2003, the disclosure of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to electrical and electronic circuits and systems. More specifically, the present invention relates to digital to analog converters.

Description of the Related Art:

Digital to analog converters are widely used for converting digital signals to analog signals for many electronic circuits. For example, a high resolution, high speed digital to analog converter (DAC) may find application in video circuits, high quality audio, instrumentation applications, and in the transmit path for high dynamic range communications applications. It may also be used in high speed analog to digital converters (ADCs) that utilize DACs such as successive approximation ADCs or subranging ADCs. There is currently a desire for faster DAC operating speed and

improved accuracy relative to conventional designs.

A common DAC, the current summing DAC, generates an analog output signal by selectively switching a number of current sources (or cells) into or out of a current summing device in response to a digital input signal. Each DAC cell includes a current source and a current steering switch, which is typically implemented using a differential pair of transistors. As the input to a particular cell is changed, the transistors might be commanded to go from on to off, or from off to on. There is a finite delay time while the transistors are changing state. This delay time is largely a function of the transistor's collector to base capacitance C_{CB}, the impedance of the driving source, and the value of the load resistance. Even though the transistors are being used as current steering transistors, they have finite gain. Therefore, the Miller effect is applied to C_{CB}, increasing the parasitic capacitance. This slows the response time of the switches, reducing the overall operating speed of the DAC.

Additionally, as the voltages on the collectors of the steering transistors vary, they are coupled (albeit considerably attenuated) to the collectors of the current sources. These attenuated voltages will impact the accuracy of the current sources. All of these perturbations must also settle to within the accuracy of the DAC. The two areas discussed above limit the speed at which the DAC can be run and the DAC's ability to meet its accuracy requirements.

Furthermore, the inputs to the DAC cells are typically driven by standard ECL (emitter-coupled logic) circuits. These circuits also have a switching delay, as well as an output voltage swing defined as being from about –0.9 V to –1.7 V. This voltage swing is larger than desired. The larger the voltage swing, the more undesirable energy is coupled into the DAC circuitry and the longer it takes to settle to the correct value.

Hence, there is a need in the art for an improved digital to analog converter having a faster operating speed and improved accuracy over prior approaches.

SUMMARY OF THE INVENTION

The need in the art is addressed by the current switch of the present invention. The novel current switch includes a differential pair of transistors Q1 and Q2, a pair of cascode transistors Q_A and Q_B coupled to Q1 and Q2, respectively, and a circuit for maintaining Q_A and Q_B in an 'on' state regardless of the states of Q1 and Q2. The circuit for keeping Q_A and Q_B on includes first and second current sources adapted to supply first and second trickle currents to the emitters of Q_A and Q_B, respectively. The bases of Q_A and Q_B are connected in common to a voltage source V_{REF4}, which, in an illustrative embodiment, is implemented using a Schottky diode for lower impedance. The circuit for driving Q1 and Q2 may also be implemented using a current switch with trickle current, cascode transistors Q14 and Q15 to further improve settling times.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic of a common conventional implementation of an integrated circuit DAC.

Fig. 2 is a simplified schematic of a conventional DAC cell switch driver.

Fig. 3 is a simplified schematic of a DAC designed in accordance with an illustrative embodiment of the teachings of the present invention.

Fig. 4 is a simplified schematic of a conventional implementation of a voltage source for supplying V_{REF4}.

Fig. 5 is a simplified schematic of a voltage source for supplying V_{REF4} to the cascode circuit, in accordance with an illustrative embodiment of the teachings of the present invention.

Fig. 6 is a simplified schematic of a DAC cell switch driver designed in accordance with an illustrative embodiment of the teachings of the present invention.

DESCRIPTION OF THE INVENTION

Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

Fig. 1 is a simplified schematic of a common conventional implementation of an integrated circuit DAC 10. Two of N current steering cells 12 and 14 are shown in the figure. In practice there will be several more cells. The number of cells N depends on the desired resolution of the DAC. Each cell 12, 14 selectively switches current between a first current summing bus 16 and a second current summing bus 18 in response to an N-bit digital input signal. For example, the first cell 12 is controlled by a signal B_1, representing the least significant bit (LSB) of the N-bit digital word, and the next cell 14 is controlled by a signal B_2, representing the next LSB. Each current summing bus 16, 18 is connected to ground through a load resistance R_L. The analog output of the DAC 10 is taken from the voltage difference between the two buses 16 and 18.

Each DAC cell 12 and 14 is thus a current switch, which is typically implemented using a differential pair of transistors (Q1, Q2 in the first cell 12, and Q3, Q4 in the second cell 14). The current to be steered is set by a current source 20 and 22, respectively. These two current sources 20 and 22 are buffered from the switching transistors Q1, Q2 and Q3, Q4 by two cascode transistors Q5 and Q7, respectively. As

shown in Fig. 1, the collector of Q1 is connected to the first bus 16, the base of Q1 is connected to B_1, and the emitter of Q1 is connected in common with the emitter of Q2 to the collector of Q5. The collector of Q2 is connected to the second bus 18, and the base of Q2 is connected to $-B_1$. Similarly, for the second cell 14, the collector of Q3 is connected to the first bus 16, the base of Q3 is connected to B_2, and the emitter of Q3 is connected in common with the emitter of Q4 to the collector of Q7. The collector of Q4 is connected to the second bus 18, and the base of Q4 is connected to $-B_2$. The bases of Q5 and Q7 are connected to a reference voltage V_{REF2}.

The current source 20 is implemented using a transistor Q6 having a base connected to a reference voltage V_{REF1}, a collector connected to the emitter of Q5, and an emitter connected to a voltage supply $-V_{CC}$ through a resistor R1. The current I_1 supplied by the current source 20 is given approximately by $I_1=(V_{REF1}-0.8+V_{CC})/R_1$. Similarly, the current source 22 is implemented using a transistor Q8 having a base connected to V_{REF1}, a collector connected to the emitter of Q7, and an emitter connected to $-V_{CC}$ through a resistor R2. The current I_2 supplied by the current source 22 is given approximately by $I_2=(V_{REF1}-0.8+V_{CC})/R_2$.

The function of the transistors Q1 and Q2 is to steer the current I_1 out of either the first bus 16 or the second bus 18 depending on the digital code input to the pair. For example, if B_1 is more positive than $-B_1$, then Q1 is turned on and Q2 off. Thus, current is steered through Q1, drawing current from the first bus 16 but not from the second bus 18. If B_1 is more negative than $-B_1$, then Q1 is turned off and Q2 on, resulting in current being drawn through Q2 from the second bus 18 but not the first bus 16. The second pair of transistors, Q3 and Q4, function the same way in response to the code B_2. In order to increase the operating speed of the DAC 10, the switching time of the transistors (Q1, Q2, Q3, Q4) needs to be reduced. One reason the switches have a slow settling time is because they are each tied to a current summing bus having a finite impedance R_L, causing the transistors to have gain. Since they have gain, they have parasitic capacitances C_{CB} located between the base and collector, and these capacitances are multiplied by the gain (Miller effect). This slows down the circuit.

Secondly, as the voltages on the current summing buses 16 and 18 change (i.e.,

the voltages ΔV on the collectors of the steering transistors), those voltages are coupled (albeit considerably attenuated) through the capacitances of the switching transistors to the collectors of the current source cascode transistors Q5 and Q7 where they are further attenuated. These attenuated voltages ($\Delta V'$) will impact the current sources Q6 and Q8, since their collector voltages ($\Delta V''$) are thus changing as a function of the voltages on the current buses 16 and 18. All of the perturbations must also settle to within the accuracy of the DAC. The two areas discussed above combine to, in part, establish the speed in which the DAC can be run and the DAC's ability to meet its accuracy requirements.

The current steering transistors Q1, Q2 and Q3, Q4 of the DAC 10 shown in Fig. 1 are typically driven by a standard ECL circuit as shown in Fig. 2. Fig. 2 is a simplified schematic of a conventional DAC cell switch driver 30. The circuit 30 includes a current switch 32 comprised of a differential pair of transistors Q10 and Q11, having emitters connected in common to a current source 34 generating a current I_S. The bases of Q10 and Q11 are connected to digital input signals X_n and $-X_n$, respectively, and the collectors are each coupled to ground through a resistor R_S. The collectors of Q10 and Q11 are connected to the bases of emitter follower transistors Q12 and Q13, respectively. The collectors of Q12 and Q13 are connected to ground, and their emitters are each connected to a current source 36 and 38, respectively. The output voltage B_n is taken at the emitter of Q13, and the output voltage $-B_n$ is taken at the emitter of Q12.

This circuit 30 has a similar problem as the DAC cells 12, 14 of Fig. 1: the current switch 32 has a defined switching delay. In addition, the lower the output impedance of the driver circuit 30, the better the combined circuits 10 and 30 perform. The output impedance of the circuit 30, however, is proportional to the resistance R_S, and there are limits on how small R_S can be. The output voltage swing is defined as being from -0.9 V to less than -1.7 V. This swing places a minimum value on R_S for a reasonable current level I_S since the minimum output voltage is less than or equal to -1.7 volts. Therefore, $I_SR_S+0.9$ V must be greater than 1.7 V. For an I_S of 0.5 mA, R_S must therefore be greater than 1.6 kΩ.

Furthermore, this drive circuit 30 results in a drive voltage that goes from -0.9

V to −1.7 V for a voltage swing of 0.8 V or greater. This voltage swing is larger than desired. The larger the voltage swing the more undesirable energy is coupled into the DAC circuitry and the longer it takes to settle to the correct value.

The present invention improves upon the prior art by introducing a novel current switch having a cascode circuit with idle or 'trickle' currents placed at the outputs of the switching transistors. These cascode circuits decrease the time required by the switching transistors to switch on and off, thereby decreasing settling time. Used in a DAC cell, the cascode circuit also isolates the switching transistors from the output summing nodes, thereby improving the DAC's overall accuracy and dynamic range. Used in a driver circuit, it also allows for the reduction of the output voltage swing without increasing the output impedance, thereby improving the overall DAC's settling time.

Fig. 3 is a simplified schematic of a DAC 50 designed in accordance with an illustrative embodiment of the teachings of the present invention. The DAC 50 includes a novel current switch or DAC cell 52 (only one cell of many is shown in the figure for simplicity). The current switch 52 includes a differential pair of transistors Q1 and Q2, whose bases are connected to complementary input signals B_1 and $-B_1$, respectively, and a current source 20 that supplies a current I_1. The current source 20 may be buffered from the switching transistors Q1, Q2 by a cascode transistor Q5, having a base connected to a reference voltage V_{REF2} and a collector connected to the common emitters of Q1 and Q2. In the illustrative embodiment, the current source 20 is implemented using a transistor Q6 having a base connected to a reference voltage V_{REF1}, a collector connected to the emitter of Q5, and an emitter connected to a voltage supply $-V_{CC}$ through a resistor R1.

In accordance with the teachings of the present invention, the current switch 52 also includes a cascode circuit 54. The cascode circuit 54 includes a pair of cascode transistors Q_A and Q_B coupled to the collectors of the switching transistors Q1 and Q2, respectively. The bases of Q_A and Q_B are connected in common to a reference voltage VREF4, and the outputs of the currents switch 52 are now taken at the collectors of QA and QB. The collector of Q_A is therefore coupled to the first current summing bus 16,

drawing a current I_A, and the collector of Q_B is coupled to the second current summing bus 18, drawing a current I_B. There is one important addition to the circuit 54 and that is the addition of the trickle current sources 56 and 58 coupled to the emitters of Q_A and Q_B, respectively.

In the illustrative embodiment, the current source 56 is implemented using a transistor Q_C having a base connected to a reference voltage V_{REF3}, an emitter connected to $-V_{CC}$ through a resistor R_C, and a collector connected to the emitter of Q_A, drawing a current I_{T1}. The current source 58 is implemented using a transistor Q_D having a base connected to V_{REF3}, an emitter connected to $-V_{CC}$ through a resistor R_D, and a collector connected to the emitter of Q_B, drawing a current I_{T2}.

Because of the addition of the trickle circuits 56 and 58, the cascode transistors Q_A and Q_B are always on. The trickle currents I_{T1} and I_{T2} hold the transistors Q_A and Q_B in the linear range of operation, even when a particular switching transistor Q1 or Q2 is turned off. This is most critical to the delay time performance of the circuit. As an example of how the circuit performs, assume $-B_1$ is more positive than B_1. This condition turns 'on' transistor Q2 and allows I_1 to be drawn from the second current bus 18. Q_1 is off and no portion of I_1 passes through from the first bus 16. It must be noted that both trickle currents I_{T1} and I_{T2} continue to be drawn through Q_A and Q_B, respectively. In this case $I_A = I_{T1}$ and $I_B = I_1 + I_{T2}$.

It is easily shown that the trickle currents will not impact the current summing accuracy of the DAC 50. Let the output voltage $V_{OUT}=V_A-V_B$. Looking at the contribution of I_{T1} and I_{T2}, $V_{OUT}=I_{T1}R_L-I_{T2}R_L-I_1R_L$, or $V_{OUT}=R_L[(I_{T1}-I_{T2})-I_1]$. If $I_{T1}=I_{T2}$, then the output would be $V_{OUT} = -R_LI_1$, the correct value. Even if I_{T1} and I_{T2} are not perfectly matched, their contribution to the output V_{OUT} is simply an offset (since it does not vary with the input code) and can be easily removed through trimming. This is accomplished when the differential offset is trimmed to zero for all the cells. The trickle currents are about 10 to 100 times smaller than I_1 and are chosen for optimum DAC performance.

By adding the cascode circuit 54 to the current switch 52, the turn on delay time for the switching transistors Q1, Q2 is significantly improved. In the prior art, the turn

on time was dominated by C_{CB}, the Miller effect, and the node impedance R_L. Now, with the improved implementation, since the transistors Q_A and Q_B are always on, the collectors of Q1 and Q2 are held at a constant voltage which is approximately V_{REF4}–0.8 V. This effectively eliminates the Miller effect. Also since the collectors of Q1 and Q2 are connected to the emitters of Q_A and Q_B, they no longer work into the impedance of the summing node of R_L. Instead, there is a much lower impedance since Q_A and Q_B are grounded base amplifiers. Between the elimination of the Miller effect and the lowering of the impedance seen by the collectors of Q1 and Q2, the turn on/turn off times of Q1 and Q2 are significantly reduced, thereby increasing the speed of operation of the DAC 50.

The second area of performance improvement involves how voltage variations on the buses 16 and 18 reflect down to the collector of the current source 20. While the magnitude of the current source 20 collector voltage is difficult to calculate exactly, it is easy to see that the cascode stages act as an additional buffer or attenuator between the buses 16 and 18 and the current source 20. This essentially eliminates bus voltage variations as a cause of current source errors.

The following table gives sample values for the components of Fig. 3:

$-V_{CC}$	- 5 V
V_{REF1}	- 2.7 V
V_{REF2}	- 1.8 V
V_{REF3}	- 3.95 V
V_{REF4}	- 0.8 V
R_1	2.4 kΩ
R_C	5 kΩ
R_D	5 kΩ
R_L	50 Ω (for a 9-bit unary, or 14-bit binary DAC)
I_1	0.624 mA

It should be pointed out that the lower the impedance of the voltage source

V_{REF4}, the more effective Q_A and Q_B become in providing the benefits described. As the V_{REF4} impedance goes to zero, any transient perturbations at the load resistance is shunted to virtual ground. This helps to isolate these dynamic settling errors from the switch pair Q1, Q2. Under normal circumstances, V_{REF4} would be implemented as shown in Fig. 4.

Fig. 4 is a simplified schematic of a conventional implementation of a voltage source 70 for supplying V_{REF4}. The voltage source 70 includes a diode D1 having an anode connected to ground and a cathode connected to a current source 72. The current source 72 is implemented using a transistor Q_V having a base connected to a reference voltage V_{REF}, an emitter connected to $-V_{CC}$ through a resistor R_V, and a collector connected to the cathode of D1. The output voltage V_{REF4} is taken at the cathode of D1. Normally, D1 would simply be another transistor connected as a diode. In accordance with the teachings of this invention, however, the diode is implemented as a Schottky diode, as shown in Fig. 5.

Fig. 5 is a simplified schematic of a voltage source 80 for supplying V_{REF4} to the cascode circuit 54, in accordance with an illustrative embodiment of the teachings of the present invention. The circuit 80 is identical to that of Fig. 4, except the diode D1 is replaced with a Schottky diode D_S. A Schottky diode has a lower on resistance, a higher transition frequency f_t, and a low impedance over a wider bandwidth than the normal diode-connected transistor. When used as the reference voltage source V_{REF4} for the cascode transistors Q_A and Q_B, its low impedance improves the cascode transistor stage's isolation and settling time.

The trickle current, cascode circuit 54 can be used in a similar manner to improve the speed of the current switch of the DAC cell switch driver. Fig. 6 is a simplified schematic of a DAC cell switch driver 90 designed in accordance with an illustrative embodiment of the teachings of the present invention. The driver 90 is similar to that of Fig. 2, except the current switch 32 is replaced with a novel current switch 92, having a trickle current, cascode circuit 94. The current switch 92 includes a differential pair of transistors Q10 and Q11, having bases connected to complementary input signals X_n and $-X_n$, respectively, emitters connected in common to a current

source 32 that supplies a current I_S, and collectors connected to the cascode circuit 94.

The cascode circuit 94 includes a pair of cascode transistors Q14 and Q15 coupled to the collectors of the switching transistors Q10 and Q11, respectively. The bases of Q14 and Q15 are connected in common to a voltage supply V_{BIAS}, the collectors of Q14 and Q15 are each connected to ground through a resistor R_S, and the emitters are each connected to a current source 96 and 98, respectively, which supply trickle currents I_{T3} and I_{T4}, respectively.

The cascode implementation with trickle currents shortens the delay time of the differential current switch 92 of the driver circuit 90, as described for the DAC cell 52 of Fig. 3. In addition, it helps to set the proper DC threshold level while maintaining a low overall output impedance, allowing for a reduction of the output voltage swing, which will reduce the voltage coupling into the DAC current steering switches, thereby improving the overall DAC's settling time.

A design example follows to illustrate the setting of the voltage range. In this example, the goal is to limit the voltage swing from −1.2 V to −1.6 V (a range of only 0.4 volts, half the range of the prior art circuit of Fig. 2), without increasing the output impedance. Assume the base of Q10 is more positive than Q11. The voltage drop across the collector resistor of Q14 is given by $R_S(I_S)+R_S(I_{T3})$. Setting $-B_n= -R_S(I_S+I_{T3})-V_{BEQ12}$ (where V_{BEQ12} is the base to emitter voltage of Q12, which is approximately 0.8 V) to −1.6 V, then $(I_S+I_{T3})=(1.6-0.8)/R_S= 0.8/R_S$. Let $R_S=1.6$ kΩ. Then $I_S+I_{T3}= 0.5$ mA. This sets the lower level of the voltage swing.

Now, let transistor Q10 turn off, and set $-B_n= -R_S(I_{T3})-0.8$ V to −1.2 V. Solving for I_{T3}, $I_{T3}=0.4$ V/1.6 kΩ=0.25 mA. Thus, if I_S is set to 0.25 mA, and I_{T3} and I_{T4} are each equal to 0.25 mA, then the combined goals of reducing the voltage swing to the input of the DAC without increasing the output impedance of the drive circuitry are met.

Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications, applications and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

Accordingly,

WHAT IS CLAIMED IS: